Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.056”**

**PAD FUNCTION:**

1. **N. Y0**
2. **N. Y1**
3. **N. Y2**
4. **N. Y3**
5. **N. Y4**
6. **N. Y5**
7. **N. Y6**
8. **N. Y7**
9. **N. Y8**
10. **N. Y9**
11. **GND**
12. **N. Y11**
13. **N. Y12**
14. **N. Y13**
15. **N. Y14**
16. **N. Y15**
17. **N. E1**
18. **N. E2**
19. **A3**
20. **A2**
21. **A1**
22. **A0**
23. **VCC**

**3 2 1 24 23**

**10 11 12 13**

**22**

**21**

**20**

**19**

**18**

**17**

**16**

**15**

**14**

**4**

**5**

**6**

**7**

**8**

**9**

**.102”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0033” X .0033”**

**Backside Potential: Vcc or LEAVE FLOATING**

**Mask Ref: HCT154T**

**APPROVED BY: DK DIE SIZE .059” X .102” DATE: 8/26/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54HCT154**

**DG 10.1.2**

#### Rev B, 7/19/02